

Exhibit B

MELVIN RAY MERCER

Independent Consultant
and
Professor Emeritus
Department of Electrical and Computer Engineering
Texas A & M University

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EDUCATION: The University of Texas at Austin, Ph.D., 1980
Stanford University, MS, 1971
Texas Tech University, BS, 1968

PROFESSIONAL REGISTRATION: Texas #62016

ACADEMIC POSITIONS:

Texas A & M University, Professor Emeritus, 2006
Texas A & M University, Professor and Chair Holder, 1/95-9/2005
University of Texas at Austin, Professor, 9/91-12/94
University of Texas at Austin, Associate Professor, 9/87-8/91
University of Texas at Austin, Assistant Professor, 1/83-8/87
University of Texas at San Antonio, Lecturer, 1977-80

OTHER PROFESSIONAL EXPERIENCE:

Independent Consultant for Mercer and Associates, Inc., Dallas, TX 1984-present
Member of Technical Staff, Bell Laboratories, Murray Hill, NJ, 1980-83
Member of Technical Staff, Hewlett-Packard Laboratories, Palo Alto, CA, 1973-77
Research/Development Engineer, GTE Sylvania, Mountain View, CA, 1968-73
(in 2000, GTE merged with Bell Atlantic to form Verizon)

CONSULTING:

Hale and Dorr, Boston, Massachusetts, Intel, 2001
Fulbright and Jaworski, Houston, TX, Emachines, 1999-2000
Akin, Gump, Strauss, Hauer & Feld, 2000
Harris Corporation, Melbourne, FL, 1999-2001
SigmaTel, Austin, TX, 1999-2000
Martin Gruppen, Denmark, 1999
AT&T, Inc., Murray Hill, NJ, 1995-98
Sematech, Inc., Austin, TX 1994
Teradyne, Inc., Boston, MA, 1993-94
Integri-Test Corp., Commack, NY 1993
Spectrum Information Technologies, Dallas, TX 1993
Motorola Semiconductor, Austin, TX, 1987-88, 1991-99
Rockwell International, Newport Beach, CA, 1991, 1995
Teltech Resource Network, Minneapolis, MN, 1986-93
Cimflex Teknowledge, Pittsburgh, PA, 1989-90
IBM, Inc., Austin, TX, 1984, 1988-90

MCC, Austin, TX, 1989
CBS, New York, NY, 1985-86
Harris Data Communications Inc., Dallas, TX, 1984-86
Cellular Technology, Inc., Lubbock, TX 1985 - 87
Attorney General's Office, State of Texas, Austin, TX, 1984
Lockheed Missiles and Space Company, Austin, TX, 1983
Rothe Development Company, San Antonio, TX, 1979

TECHNOLOGY BASED BUSINESS EXPERIENCE:

Founder, Technical Advisor, and Owner of Conference Management Services, Inc., 1993 – 2013
Technical Advisory Board Member, Test Systems Strategies, Inc., Beaverton, OR, 1988-93
Advisor and Survey Developer, IBM, Inc., Austin, TX, 1988-90
Advisor, Early Cellular Telephone Minority Carriers, Lubbock, Texas, 1983 - 1987

HONORS AND AWARDS:

National and International:

Fellow of the Institute of Electrical and Electronics Engineers, 1994
National Science Foundation -- Presidential Young Investigator, 1986
Best Paper Award, VLSI Test Conference, Dana Point, CA, 1999
Best Paper Award, Design Automation Conference, San Francisco, CA, 1991
Best Paper Award, International Test Conference, Philadelphia, PA, 1982
Best Paper Award, Honorable Mention, Int. Test Conference, Washington, DC, 1988
Texas Tech Electrical Engineering Academy, Lubbock, Texas, 1999
Who's Who in America, 48th, 49th, 50th, 56th, 58th, 59th, 63rd, 67th and 69th Editions, 1994, 1995, 1996, 2000, 2002, 2004, 2005, 2009, 2012, and 2015
Who's Who in American Education, 3rd Edition, 1992-1993
Who's Who in America Finance and Industry, 31st Edition, 1999
Who's Who of Emerging Leaders in America, 7th Edition, 1990 & 1992
Who's Who in Science and Engineering, 3rd, 4th, 7th, 9th & 10th Editions, 2003-2009
Who's Who in the South and Southwest, 21st, 22nd, 23rd, 24th, 37th, 38th, 40th & 41st Editions, 1988, 1990, 1992, 1995, 2011, 2012, 2013, 2014, & 2015
Who's Who in the World, 10th, 11th, 17th, and 21st Editions, 1991, 1992, 2000 & 2004
Meritorious Service Award, IEEE Computer Society, 1993
Faculty Nominator and Advisor for Jennifer Dworak – Recipient of a National Science Foundation Graduate Research Fellowship 2000 – 2003
Co-Author and Advisor for Jennifer Dworak and Amy Wang – Recipient of the “IEEE Test Technology Technical Council Naveena Nagi Award for 2004” presented in Napa Valley, California

Local:

Computer Engineering Chair in Electrical Engineering, A&M, 1995-2005
Faculty Nominator and Advisor for Jennifer Dworak – Recipient of The Ethel Ashworth-Tsutsui Memorial Award for Graduate Student Research 2002
Texas A&M Outstanding Masters Thesis Award: Jennifer Dworak, 1999-2000
Listed in the Texas A&M Center for Teaching Excellence 2002 Eagle Award Booklet, May 3, 2002
Temple Foundation Endowed Professorship #3 in Engineering, UT, 1991-94
Engineering Foundation Endowed Faculty Fellowship in Engineering, UT, 1990-91
Werner W. Dornberger Centennial Teaching Fellowship in Engineering, UT, 1984-90
Engineering Foundation Faculty Award, UT, 1986
Outstanding Doctoral Dissertation: Honorable Mention, T. E. Kirkland, UT, 1986-87
MCC Sponsored Outstanding Student Paper Award: Bill Underwood, 1991-92
High School Valedictorian

PROFESSIONAL SOCIETIES AND ACTIVITIES:

Government:

National Science Foundation Advisory Committee for Microelectronic Information Processing Systems (MIPS), 1987-88
National Science Foundation Engineering Initiation Awards Evaluation Panel Member —Design, Tools and Test Program, 1987 and 1993
National Science Foundation Advisory Workshops
 Future of Testing and Design for Testability, June 30, 1989
 Future of VLSI and Computer-Aided Design, October 15-16, 1992
Presentation to the Texas State Board of Registration for Professional Engineers on Computer Engineering and suitable criteria for registration, 1985

Journals and Archival Publications:

Guest Editor, Special Issue on Design for Testability, *IEEE Design and Test of Computers*, October, 1986
Editor, Design for Testability, *IEEE Design and Test of Computers*, 1985-88
Guest Editor, *IEEE Transactions on Computer-Aided Design of Circuits and Systems*, 1988
Guest Editor, Special Issue on 1989 International Test Conference, *IEEE Design and Test of Computers*, April 1990.
Editorial Board Member, *Journal of Electronic Testing: Theory and Applications*, 1990-92
Editorial Advisory Board, *Microelectronics Journal: Circuits and Systems*, 2000 – 2003

Conferences and Workshops:

Finance Chair, Third IEEE Workshop on Microprocessor Test and Verification, (MTV'02), 2002
Program Committee, Ninth IEEE International Test Synthesis Workshop, (ITSW), 2002
Program Committee, Second IEEE Workshop on Microprocessor Test and Verification, (MTV 99), 1999
Exhibits Chairman, Fault-Tolerant Computing Symposium 1994
Planning Chairman, International Test Conference, 1992-93
Marketing Vice-Chairman, International Test Conference, 1990
Program Chairman, International Test Conference, 1989
Program Vice-Chairman, International Test Conference, 1988
Steering Committee, International Test Conference, 1987-93
Program Committee, International Test Conference, 1986-89
Program Committee, IEEE Design for Testability Workshop, 1988-96
Program Committee, International Conference on Computer-Aided Design, 1987
Program Committee, First MCC-University Research Symposium, Austin, TX, 1987

Local Offices:

Vice-Chairman, Central Texas Chapter, IEEE Computer Society, 1983-85
Chairman, Central Texas Chapter, IEEE Computer Society, 1985-86

Memberships:

Institute of Electrical and Electronics Engineers (IEEE), Fellow 1994, Life Member 2012

TEXAS A & M UNIVERSITY COMMITTEE ASSIGNMENTS:

City/County Committees:

Bryan/College Station Economic Development Group
Marketing Committee for the Information Technology Task Force, 1999

University Committees:

Search Committee -- Associate Provost for Information Technology, 1997-99
Research Infrastructure Committee, 1998-99

College of Engineering Committees:

Computer Engineering Committee, Chairman, 2002
Tenure and Promotion Committee, 2000 - 2002
Computer Engineering Committee, Chairman, 1996-1999
Chair Holders Committee, 1995-
Compaq Liaison Committee 1996-
Computer Science Department Head Search Committee, 1996-98
ABET Review Committee, Computer Engineering, 1995

ABET Review Committee, Computer Engineering, Chair, 1998
Ad Hoc Committee to Study the Merger of the CS and EE Departments, 1996
PAM Advisory Committee, 1995-96
Spencer J. Buchanan Professorship Review Committee, 1997

Departmental Committees:

Computer Engineering Area Leader, 1995-present
Faculty Search Committee for the Computer Engineering Group, Chairman, 1995-present
Teaching Assignments for the Computer Engineering Group, 1995-present
Tenure and Promotion Committee, 1996-98, 2000-02, 2003-2005
Graduate Studies Committee, 1996-present
Faculty Advisory Committee, 1997-99
Strategic Planning Committee, 1998
Search Committee for the Eugene Webb Professorship, 1998-99
Search Committee for the Texas Instruments Jack Kilby Chair in Analog Engineering, 1998-99

UNIVERSITY OF TEXAS COMMITTEE ASSIGNMENTS:

University Committees:

Presentation to the MCC Site Selection Committee, the MCC Fact Finding Committee,
and the MCC Technology Advisory Board, 1983
Science and Engineering Development Program Review for Dr. Thomas Everhart
and Dr. Frank Press, National Academy of Sciences, 1984
Parking and Traffic Panel of the General Faculty, 1983-85
Hearing Officer for Faculty Grievances, 1987-88
University Council Representative, 1992-94
University Faculty Senate, 1992-94
Faculty Governance Committee, 1992-93

College of Engineering Committees:

Scholastic Appeals Committee, 1983-84
Ad Hoc Committee to Prepare a DOD Proposal for a Software Engr. Institute, 1984
State Agency Research Forum Speaker, May 10, 1984
Continuing Engineering Studies Committee, 1984-85
Ad Hoc Committee on Microelectronics and Computer Engineering, 1983-85
Presentation to Heads of State Agencies and Selected Federal Personnel, 1985
Computer Committee, 1985-86
GEC Faculty Meritorious Service Award Committee, 1987
Presentation to Industrial Representatives Research Forum, April 30, 1987
Undergraduate Degree Program Evaluation, 1986-88
Continuing Engineering Studies Committee, 1986-88
Televised Instruction Committee, 1987-91
Briefing for AT&T Visitors, November 21, 1991

Departmental Committees:

Committee on CAD/CAM and Advanced Graphics, 1983
Chairman, MCC Graduate Fellowships Recruiting Poster Committee, 1984
Microelectronics and Computer Engineering Research Support Committee, 1984
Chairman, Computation, Word Processing, and Telecom. Committee, 1984-85
Chairman, Industrial Liaison Committee, 1985-86
Computation, Word Processing, and Telecommunications Committee, 1985-86
Equipment Committee, 1984-86
ABET Accreditation for ECE in Computer Engineering (Site Visit), 1987
VLSI Course Area Committee, 1986-87
Chairman, Local Area Network Committee, 1987-88
Search Committee for New ECE Chairman, 1988-89
ECE Visiting Committee, 1989-90
Chairman, Annual Research Review Committee, 1988-92

Graduate Student Recruitment at Stanford University, January 1992
Alumni Committee 1992-93
Computer Engineering Research Center Executive Committee, 1988-93
Computer Sciences Liaison, 1988-93
Digital Systems Course Area Committee, 1988-93
Chairman, Teaching Effectiveness Committee, 1991-94
Budget Council, 1991-94
Computer Engineering Representative to the ECE Area Committee 1993-94
Junior Faculty Recruiting Committee, Computer Engineering, 1985-94

PUBLICATIONS:

Refereed Conference and Archival Journal Publications:

M. R. Mercer and V. D. Agrawal, "A Novel Clocking Technique for VLSI Circuit Testability," *IEEE Journal of Solid-State Circuits*, Vol. SC-19, April 1984, pp. 207-212.

K. S. Hwang and M. R. Mercer, "Derivation and Refinement of Fanout Constraints to Generate Tests in Combinational Logic Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, October 1986, pp. 564-572.

T. Kirkland and M. R. Mercer, "Automatic Test Pattern Generation Algorithms," *IEEE Design and Test of Computers*, June 1988, pp. 43-55.

E. S. Park, M. R. Mercer, and T. W. Williams, "A Statistical Model for Delay-Fault Testing," *IEEE Design and Test of Computers*, February 1989, pp. 45-55. { NSF, ONR }

D. E. Ross, K. M. Butler, and M. R. Mercer, "Exact Ordered Binary Decision Diagram Size When Representing Classes of Symmetric Functions," *Journal of Electronic Testing: Theory and Applications*, vol. 2, no. 3, August 1991, pp. 243-259. { NSF }

E. S. Park, M. R. Mercer, and T. W. Williams, "The Total Delay Fault Model and Statistical Delay Fault Coverage," *IEEE Transactions on Computers*, vol. 41, no. 6, June 1992, pp. 688-698. { NSF, ONR }

E. S. Park and M. R. Mercer, "An Efficient Delay Test Generation System for Combinational Logic Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 11, no. 7, July 1992, pp. 926-938. { NSF, ONR, TATP }

R. Kapur and M. R. Mercer, "Bounding Signal Probabilities for Testability Measurement Using Conditional Syndromes," *IEEE Transactions on Computers*, vol. 41, no. 12, December 1992, pp. 1580-1588. { NSF, ONR, SRC }

M. Heap and M. R. Mercer, "Least Upper Bounds on OBDD Sizes," *IEEE Transactions on Computers*, accepted for publication, July 1993.

C. Oh and M. R. Mercer, "Efficient Logic-Level Timing Analysis Using Constraint-Guided Critical Path Search," *IEEE Transactions on VLSI*, September 1996. { ONR }

J. Dworak, J. Wicker, S. Lee, M. R. Grimaila, K. M. Butler, B. Stewart, L-C. Wang, and M. R. Mercer, "Defect-Oriented Testing and Defective-Part-Level Prediction," *IEEE Design and Test of Computers*, January-February, 2001, Vol. 18, No. 1, pp. 31 - 41. { SRC, NSF, TATP }

M. R. Mercer, V. D. Agrawal and C. M. Roman, "Test Generation for Highly Sequential Scan-Testable Circuits through Logic Transformation," *International Test Conference 1981*, Philadelphia, PA, October 1981, pp. 561-565.

V. D. Agrawal and M. R. Mercer, "Testability Measures -- What Do They Tell Us?," *International Test Conference 1982*, Philadelphia, PA, November 1982, pp. 391-396. **(Best Paper of the 1982 ITC)**

M. R. Mercer and B. Underwood, "Correlating Testability with Fault Detection," *International Test Conference 1984*, Philadelphia, PA, October 1984, pp. 697-704.

E. Schell and M. R. Mercer, "CADTOOLS: A CAD Algorithm Development System," *The ACM/IEEE Design Automation Conference (22nd) Proceedings*, Las Vegas, NV, June 23-26, 1985, pp. 658-666.

J. Salick and M. R. Mercer, "Built-In Self Test Input Generator for Programmable Logic Arrays," *International Test Conference 1985*, Philadelphia, PA, November 1985, pp. 115-125.

K. S. Hwang and M. R. Mercer, "Derivation and Refinement of Fanout Constraints to Generate Tests in Combinational Logic Circuits," *IEEE International Conference on Computer-Aided Design*, Santa Clara, CA, November 1985, pp. 10-12.

K. S. Hwang and M. R. Mercer, "Informed Test Generation Guidance Using Partially Specified Fanout Constraints," *1986 International Test Conference*, Washington, DC, September 8, 1986, pp. 113-119.

R. K. Gaede, M. R. Mercer and B. Underwood, "Calculation of Greatest Lower Bounds Obtainable by the Cutting Algorithm," *1986 International Test Conference*, Washington, DC, September 9, 1986, pp. 498-505.

M. R. Mercer, "Logic Elements for Universally Testable Circuits," *1986 International Test Conference*, Washington, DC, September 9, 1986, pp. 493-497.

T. E. Kirkland and M. R. Mercer, "A Two Level Guidance Heuristic for ATPG," *IEEE Fall Joint Computer Conference*, Dallas, TX, November 2-6, 1986, pp. 841-847.

B. Underwood, J. Salick, M. R. Mercer and J. Kuban, "An Automatic Test Pattern Generation Algorithm for PLAs," *IEEE International Conference on Computer-Aided Design*, Santa Clara, CA, November 10-13, 1986, pp. 152-155.

T. Kirkland and M. R. Mercer, "A Topological Search Algorithm for ATPG," *The ACM/IEEE Design Automation Conference (24th) Proceedings*, Miami, FL, June 28-July 1, 1987, pp. 502-508.

S. P. Smith, M. R. Mercer and B. Brock, "Demand Driven Simulation: BACKSIM," *The ACM/IEEE Design Automation Conference (24th) Proceedings*, Miami, FL, June 28-July 1, 1987, pp. 181-187.

E. J. Aas and M. R. Mercer, "Algebraic and Structural Computation of Signal Probability and Fault Detectability in Combinational Circuits," *Proceedings of the 17th International Symposium on Fault-Tolerant Computing*, Pittsburgh, PA, July 6-8, 1987, pp. 72-77.

D. E. Ross and M. R. Mercer, "WAVE, A Concurrent Approach to Combinational Test Pattern Generation," *Proceedings of the MCC-University Research Symposium*, Austin, TX, July 14, 1987.

E. S. Park and M. R. Mercer, "Robust and Nonrobust Tests for Path Delay Faults of a Combinational Circuit," *Proc. 1987 International Test Conference*, Washington, DC, September 1-3, 1987, pp. 1027-1034.

S. P. Smith, B. Underwood and M. R. Mercer, "An Analysis of Several Approaches to Circuit Partitioning for Parallel Logic Simulation," *Proc. 1987 IEEE International Conference on Computer Design*, Rye Brook, NY, October 5-8, 1987, pp. 664-667.

C. T. Glover and M. R. Mercer, "A Method of Delay Fault Test Generation," *Proc. 25th ACM/IEEE Design Automation Conference*, Anaheim, CA, June 13-15, 1988, pp. 90-95.

R. K. Gaede, M. R. Mercer, K. M. Butler, and D. E. Ross, "CATAPULT: Concurrent Automatic Testing Allowing Parallelization and Using Limited Topology," *Proc. 25th ACM/IEEE Design Automation Conference*, Anaheim, CA, June 13-15, 1988, pp. 597-600.

E. S. Park, M. R. Mercer, and T. W. Williams, "Statistical Delay Fault Coverage and Defect Level for Delay Faults," *Proc. 1988 International Test Conference*, Washington, DC, September 12-14, 1988, pp. 492-499. **(Honorable Mention for Best Paper of the 1988 ITC)**

S. P. Smith, B. Underwood, and M. R. Mercer, "D3FS: Demand Driven Time First Deductive Fault Simulation," *Proc. 1988 International Test Conference*, Washington, DC, September 12-14, 1988, pp. 582-592.

C. T. Glover and M.R. Mercer, "A Deterministic Approach to Adjacency Testing for Delay Faults," *Proc. 26th ACM/IEEE Design Automation Conference*, Las Vegas, NV, June 25-29, 1989, pp. 351-356.

E. S. Park and M.R. Mercer, "An Efficient Delay Test Generation System for Combinational Logic Circuits," *Proc. 27th ACM/IEEE Design Automation Conference*, Orlando, FL, June 24-28, 1990, pp. 522-528.

K. M. Butler and M.R. Mercer, "The Influences of Fault Type and Topology on Fault Model Performance and the Implications to Test and Testable Design," *Proc. 27th ACM/IEEE Design Automation Conference*, Orlando, FL, June 24-28, 1990, pp. 673-678. {NSF, SRC}

D. E. Ross, K. M. Butler, R. Kapur, and M. R. Mercer, "Fast Functional Evaluation of Candidate OBDD Variable Orderings," *Proc. of The European Conference on Design Automation*, Amsterdam, The Netherlands, February 25-28, 1991, pp. 4-10. {NSF, ONR, SRC}

R. Kapur, K. M. Butler, D. E. Ross, and M. R. Mercer, "On Bridging Fault Controllability and Observability and Their Correlations to Detectability," *Proc. of The European Test Conference*, Munich, Germany, April 10-12, 1991, pp. 333-339. {NSF, ONR, SRC}

K. M. Butler and M. R. Mercer, "Quantifying Non-Target Defect Detection by Target Fault Test Sets," *Proc. of The European Test Conference*, Munich, Germany, April 10-12, 1991, pp. 91-100. {NSF, SRC}

T. W. Williams, B. Underwood, and M. R. Mercer, "The Interdependence Between Delay-Optimization of Synthesized Networks and Testing," *Proc. 28th ACM/IEEE Design Automation Conference*, San Francisco, California, June 17-19, 1991, pp. 87-92. **(Best Paper Award at 1991 DAC)** {none}

K. M. Butler, D. E. Ross, R. Kapur, and M. R. Mercer, "Heuristics to Compute Variable Orderings for Efficient Manipulation of Ordered Binary Decision Diagrams," *Proc. 28th ACM/IEEE Design Automation Conference*, San Francisco, California, June 17-19, 1991, pp. 417-420. {NSF, ONR, SRC}

E. S. Park, B. Underwood, T. W. Williams, and M. R. Mercer, "Delay Testing Quality in Timing-Optimized Designs," *Proc. 1991 International Test Conference*, Nashville, TN, October 28 - November 1, 1991, pp. 897-905. {NSF, ONR, TATP}

K. M. Butler, R. Kapur, D. E. Ross, and M. R. Mercer, "The Roles of Controllability and Observability in Design for Test," *Proc. 1992 IEEE VLSI Test Symposium*, Atlantic City, New Jersey, April 6-9, 1992. {NSF, ONR, SRC}

M. R. Mercer, R. Kapur, and D. E. Ross, "Functional Approaches to Generating Orderings for Efficient Symbolic Representations," *Proc. 29th ACM/IEEE Design Automation Conference*, Anaheim, California, June 9-11, 1992, pp. 624-627. {NSF, ONR, SRC}

R. Kapur, J. Park, and M. R. Mercer, "All Tests for a Fault are Not Equally Valuable for Defect Detection," *Proc. 1992 International Test Conference*, Baltimore, MD, September 20-24, 1992, pp. 762-769. {NSF, ONR, SRC}

M. A. Heap, W. A. Rogers, and M. R. Mercer, "A Synthesis Algorithm for Two-Level XOR Based Circuits," *Proc. IEEE International Conference on Computer Design*, Cambridge, MA, October 11-14, 1992, pp. 459-462. {TARP}

R. B. Brashear, D. R. Holberg, M. R. Mercer and L. Pillage, "ETA: Electrical-Level Timing Analysis," *IEEE International Conference on Computer-Aided Design*, Santa Clara, CA, November 8-12, 1992, pp. 258-262. {IBM, MOTO, ONR, SRC, TATP}

J. Park and M. R. Mercer, "An Efficient Symbolic Design Verification System," *Proc. IEEE International Conference on Computer Design*, Cambridge, MA, October 3-6, 1993, pp. 294-298. {SRC}

Eun Sei Park, and M. R. Mercer, "Switch-Level ATPG Using Constraint-Guided Line Justification," *Proc. 1993 International Test Conference*, Baltimore, MD, October 17-21, 1993, pp. 616-625. {none}

R. B. Brashear, N. Menezes, C. Oh, L. Pillage, and M. R. Mercer, "Predicting Circuit Performance Using Circuit-Level Statistical Timing Analysis," *Proc. of The European Design and Test Conference*, Paris, France, February 28-March 3, 1994. {ARPA, ONR, SRC}

J. Park, M. Naivar, R. Kapur, M. R. Mercer, and T. W. Williams, "Limitations in Predicting Defect Level Based on Stuck-at-Fault Coverage," *Proc. 1994 IEEE VLSI Test Symposium*, Cherry Hill, NJ, April 25-28, 1994, pp. 186-191. {ONR, SRC}

L-C Wang, M. R. Mercer, and T. W. Williams, "Enhanced Testing Performance via Unbiased Test Sets," *Proc. of The European Design and Test Conference*, Paris, France, March 6-9, 1995, pp. 294-302. {SRC}

J. Park, C. Oh, and M. R. Mercer, "Improved Sequential ATPG Using Functional Observation Information and New Justification Methods," *Proc. of The European Design and Test Conference*, Paris, France, March 6-9, 1995, pp. 262-266. {ARPA, SRC}

L-C. Wang, Sophia Kao, M. R. Mercer, and T. W. Williams, "On the Decline of Testing Efficiency as Fault Coverage Approaches 100%," *Proc. 1995 IEEE VLSI Test Symposium*, Princeton, NJ, April 30- May 3, 1995, pp. 74 - 83. {ONR, SRC}

C. Oh and M. R. Mercer, "Efficient Timing Analysis Using Constraint-Guided Critical Path Search," *Proc. Eighth Annual IEEE ASIC Conference and Exhibit*, Austin, TX, Sept. 18 - 20, 1995, pp. 289 - 293. {ARPA, ONR}

L-C. Wang, M. R. Mercer, and T. W. Williams, "On Efficiently and Reliably Achieving Low Defective Part Levels," *Proc. 1995 International Test Conference*, Washington, DC, October 23 - 25, 1995, pp. 616-625. {SRC, ONR}

T. W. Williams, R. Kapur, M. R. Mercer, R. H. Dennard, and W. Maly, "IDDQ Testing for High Performance CMOS -- The Next Ten Years," *Proc. of The European Design and Test Conference*, Paris, France, March 11-13, 1996, pp. 578-583. {none}

L-C. Wang and M. R. Mercer, "A Better ATPG Algorithm and Its Design Principles," *Proc. 1996 International Conference on Computer Design*, Austin, TX, October 7 - 9, 1996, pp. 248-253. {SRC}

J. Park and M. R. Mercer, "Using Functional Information and Strategy Switching in Sequential ATPG," *Proc. 1996 International Conference on Computer Design*, Austin, TX, October 7 - 9, 1996, pp. 254-260. {SRC}

L-C. Wang, M. R. Mercer, and T. W. Williams, "Using Target Faults to Detect Non-Target Defects," *Proc. 1996 International Test Conference*, Washington, DC, October 22 - 24, 1996, pp. 629-638. {SRC}

T. W. Williams, R. H. Dennard, R. Kapur, M. R. Mercer, and W. Maly, "IDDQ Test: Sensitivity Analysis of Scaling," *Proc. 1996 International Test Conference*, Washington, DC, October 22 - 24, 1996, pp. 786-792. {none}

M. R. Grimaila, S. Lee, J. Dworak, K. M. Butler, B. Stewart, H. Balachandran, B. Houchins, V. Mathur, J. Park, L-C. Wang, and M. R. Mercer, "REDO -- Random Excitation and Deterministic Observation -- First Commercial Experiment," *Proc. 1999 IEEE VLSI Test Symposium*, Dana Point, Calif., April 25 - 29, 1999, pp. 268-274. **(Best Paper Award at 1999 VLSI Test Symposium)** {TATP}

J. Dworak, M. R. Grimaila, S. Lee, L-C. Wang, and M. R. Mercer, "Modeling the Probability of Defect Excitation for a Commercial IC with Implications for Stuck-at Fault-Based ATPG Strategies," *Proc. 1999 International Test Conference*, Atlantic City, NJ, September 28 - 30, 1999, pp. 1031-1037. {TATP}

R. Mehler and M. R. Mercer, "Multi-level Logic Minimization Through Fault Dictionary Analysis," *Proceedings of the 1999 International Conference on Computer Design*, Austin, TX, October 10 - 13, 1999, pp. 315-318.

J. Dworak, M. R. Grimaila, S. Lee, L-C. Wang, and M. R. Mercer, "Enhanced DO-RE-ME Based Defect Level Prediction Using Defect Site Aggregation -- MPG-D," *Proceedings of the 2000 International Test Conference*, Atlantic City, NJ, October 3 - 5, 2000, pp. 930-939. {TATP}

J. Dworak, M. R. Grimaila, B. Cobb, T-C. Wang, Li-C. Wang, and M. R. Mercer "On the Superiority of DO-RE-ME / MPG-D Over Stuck-at-Based Defective Part Level Prediction," *Proceedings of the Ninth Asian Test Symposium*, Taipei, Taiwan, December 4-6, 2000, pp. 151-157. {NSF, TATP}

T. W. Williams, M. R. Mercer, J. P. Mucha, and R. Kapur, "Code Coverage, What Does It Mean in Terms of Quality?" *Proceedings of the 2001 Annual Reliability and Maintainability Symposium*, Philadelphia, PA, January 22-25, 2001, pp. 420-424. {none}

S. Lee, B. Cobb, J. Dworak, M. R. Grimaila, and M. R. Mercer, "A New ATPG Algorithm to Limit Test Set Size and Achieve Multiple Detections of all Faults," *Proceedings of Design Automation and Test In Europe -- DATE 2002*, Paris, France, March 4 - 8, 2002, pp. 94 - 99. {SRC, NSF}

J-J Liou, Li-C Wang, K-T Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Enhancing Test Efficiency for Delay Fault Testing Using Multiple-Clocked Schemes," *Proceedings of The 39th Design Automation Conference*, New Orleans, Louisiana, June 10 - 14, 2002, pp. 371 - 374.

J.-J. Liou, L.-C. Wang, K.-T. Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Analysis of Delay Test Effectiveness with a Multiple-Clock Scheme," *Proc. 2002 International Test Conference*, Baltimore, MD, October 8 - 10, 2002, pp. 407 - 416.

J. Dworak, J. Wingfield, B. Cobb, S. Lee, Li-C Wang, and M. R. Mercer, "Fortuitous Detection and its Impact on Test Set Sizes Using Stuck-at and Transition Faults," *Proceedings of the 2002 International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT 2002)*, Vancouver, Canada, November 6-8, 2002, pp. 177 - 185.

Li-C. Wang, A. Krstic, L. Lee, K-T. Cheng, M. R. Mercer, T. W. Williams, and M. S. Abadir, "Using Logic Models to Predict the Detection Behavior of Statistical Timing Defects," *Proceedings of the 2003 International Test Conference*, Charlotte, NC, September 30 - October 2, 2003, pp.1041 - 1050.

Y. Tian, M. R. Grimaila, W. Shi, and M. R. Mercer, "Minimizing Defect Levels Using a Linear Programming Based Optimal Test Selection Method," *Proceedings of the 2003 Asian Test Symposium*, Xi'an, P. R. China, November 17 - 19, 2003.

J. Wingfield, J. Dworak, and M. R. Mercer, "Function-Based Dynamic Compaction and its Impact on Test Set Sizes," *Proceedings of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston, MA, November 3 - 5, 2003, pp. 167 - 174.

J. Dworak, J. Wingfield, B. Cobb, and M. R. Mercer, "Balanced Excitation and its Effect on the Fortuitous Detection of Dynamic Defects," *Proceedings of Design Automation and Test In Europe – DATE 2004*, Paris, France, February 16 -20, 2004, pp. 1,066 – 1,071.

J. Dworak, D. Dorsey, A. Wang, and M. R. Mercer, "Excitation, Observation, and ELF-MD: Optimization Criteria for High Quality Test Sets," *Proceedings of the 2004 IEEE VLSI Test Symposium (VTS'04)*, Napa Valley, CA, USA, April 25th - April 29th, 2004, pp. 9 - 15. **(IEEE Test Technology Technical Council Naveena Nagi Award for 2004)**

J. Dworak, J. Wingfield, and M. R. Mercer, "A Preliminary Investigation of Observation Diversity for Enhancing Fortuitous Detection of Defects," *Proceedings of the 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes, France, October 11 - 13, 2004, pp. 460 - 468.

Chapters and Books:

K. M. Butler and M. R. Mercer, *Assessing Fault Model and Test Quality*, Kluwer Academic Publishers, 1991, ISBN 0 - 7923 - 9222 - 1.

V. D. Agrawal and M. R. Mercer, "Testability Measures -- What Do They Tell Us?," in *VLSI Testing and Validation Techniques*, IEEE Tutorial, H. Reghbati, editor, 1985, pp. 401-406.

Technical Reports:

M. R. Mercer and V. D. Agrawal, "Use of Clock Signal Redundancy for Testability," Bell Laboratories Technical Memorandum, July 1981.

C. M. Roman, V. D. Agrawal and M. R. Mercer, "An LSI Chip Designed for Testability," *Proceedings of the Bell System Conference on Electronic Testing*, Princeton, NJ, September 1981.

M. R. Mercer and V. D. Agrawal, "Applications for Testability Measures in VLSI Design," *Proceedings of the Bell System Conference on Electronic Testing*, Princeton, NJ, October 1982, pp. 52-58.

M. R. Mercer, "Computer Aided Design of Digital Systems," *Discovery -- Research and Scholarship at The University of Texas at Austin*, Vol. 9, No. 3, 1985, pp 17-21.

M. R. Mercer, "Testing and Design Verification of Electronic Components -- a Perspective of the Last 40 Years," *IEEE Computer, (Invited Publication for the 40th Anniversary Issue)*, September, 1991.

Other publications:

J. Dworak, D. Dorsey, A. Wang, and M. R. Mercer with IBM Technical Contact M. W. Mehalic, "Estimating Mean Time to Failure in Digital Systems Using Manufacturing Defective Part Level," *4th Annual IBM Austin Center for Advanced Studies Conference*, Austin, TX, February 21, 2003.

PROFESSIONAL SOCIETY PRESENTATIONS:

"Testability Strategies for Custom Polycell Designs," Computer Elements Workshop on VLSI Debug and Diagnosis, IEEE Computer Society, New York, NY, May 1982.

"Interpretations of Testability Measures," IEEE Design Automation Workshop, Michigan State University, East Lansing, MI, October 1982.

"Testability Measures -- What Do They Tell Us?," Automatic Testing and Measurement Exhibition, Wiesbaden, West Germany, March 1983 (by invitation as part of the "Best of Cherry Hill" Session).

"Testing Issues at the University of Texas," International Test Conference 1983, Philadelphia, PA, October 1983.

"Refinement of Statistical Evaluation of Testability Algorithms," (with B. Underwood), Seventh Annual IEEE Workshop on Design for Testability, Vail, CO, April 1984.

"SUBTLE -- A New Methodology for Structured Testability," Seventh Annual IEEE Workshop on Design for Testability, Vail, CO, April 1984.

"Why Calculating Observability is More Difficult than Controllability," Eighth Annual IEEE Workshop on Design for Testability, Vail, CO, April 1985.

"Automatic Test Pattern Generation for PLA's," (with J. Salick and B. Underwood), Fifth Annual IEEE West Coast Testing Workshop, Lake Tahoe, CA, April 1986.

"A Method for Empirical Evaluation of the Cutting Algorithm," (with R. Gaede), 9th Annual IEEE Workshop on Design for Testability, Vail, CO, May 1986.

"Exact Calculation of Fault Detection Probabilities in Multi-Output Combinational Circuits," (with E. Aas), Built-In Self-Test Workshop, Kiawah Island, Charleston, SC, March 11-13, 1987.

"Fault Model Comparisons and a Method for Testing with Vector Pairs," (with T. Glover), 10th Annual IEEE Workshop on Design for Testability, Vail, CO, April 23, 1987.

"A Review of Current Methods in Automatic Test Pattern Generation and Design for Testability," Nordic Workshop on Testing, Roros, Norway, March 15, 1988.

"An Empirical Comparison of Random-Pattern Testability under Two Classes of Delay Fault Coverage," (with T. Glover), 11th Annual IEEE Workshop on Design for Testability, Vail, CO, April 21, 1988.

"A Novel Segmentation Scheme for Pseudo-Exhaustive Testing," (with B. Stewart), 12th Annual IEEE Workshop on Design for Testability, Vail, CO, April 20, 1989.

"Distributed Demand-Driven Logic Simulation," (with S.P. Smith), International Workshop on CAD Accelerators, Oxford University, UK, September 21, 1989.

"Syndrome Estimation in Combinational Circuits Using Conditional Probabilities," (with R. Kapur), Built-In Self-Test Workshop, Kiawah Island, Charleston, SC, March 22, 1990.

"On Evaluating Target Fault Models and Non-Target Fault Detection," (with K. Butler), 13th Annual IEEE Workshop on Design for Testability, Vail, CO, April 17, 1990.

"Testing and Design Verification -- a Functional Perspective," (**invited plenary presentation**), The International Conference on Computer Design, Cambridge, Mass., Sept. 17, 1990.

"Ordered Partial Decision Diagrams and their Applications," (with D. Ross), 14th Annual IEEE Workshop on Design for Testability, Vail, CO, April 17, 1991.

"Delay-Optimization of Synthesized Networks and its Impact on Testing," (with B. Underwood and T. W. Williams), 14th Annual IEEE Workshop on Design for Testability, Vail, CO, April 17, 1991.

"Enhanced Non-Target Defect Detection Based Upon Refined Test Sets for Target Faults," (with R. Kapur and J. Park), 15th Annual IEEE Workshop on Design for Testability, Vail, CO, April 23, 1992.

"A Comparison of Non-Target Defect Levels for Scanned and Non-Scanned Sequential Circuits When the Fault Coverage is 100%," (with J. Park and R. Kapur), 15th Annual IEEE Workshop on Design for Testability, Vail, CO, April 23, 1992.

"Testing and Design Verification -- a Functional Perspective," (**invited presentation**), The Canadian Workshop on New Directions in Testing, Montreal, Quebec, Canada, May 21, 1992.

"Design for Testability and Built-In Self-Test -- Obstacles and Opportunities," (**invited Keynote**), IEEE Workshop on Design for Testability and Built-In Self-Test, Vail, CO, April 20, 1994.

"Limitations in Predicting Defect Level Based on Stuck-at-Fault Coverage," (with J. Park, Mark Naiver, T. Williams, and R. Kapur), 15th Annual IEEE Workshop on Design for Testability, Vail, CO, April 20, 1994.

"Enhancing Testing Efficiency by Reducing Testing Biases," (with L-C. Wang, and T. W. Williams), IEEE Workshop on Design for Testability, Vail, CO, April 25, 1996.

"On Bridging Defects which Manifest as Delay Faults but are *NOT* IDDQ Testable," (with D. Ross, and G. Tu), IEEE Workshop on Design for Testability, Vail, CO, April 25, 1996.

"IDDQ Test: Sensitivity Analysis of Scaling," (with T. W. Williams, R. Kapur, R. Dennard, and W. Maly), IEEE Workshop on Design for Testability, Vail, CO, April 25, 1996.

"High Fault Coverage Behavioral Test Generation," (with L-C. Wang, and T. W. Williams), IEEE European Test Workshop, Montpellier, France, June 12 - 14, 1996.

"Failure Prediction Quality for Voltage versus IDDQ Testing Methods," (with R. Kapur and T. W. Williams), IEEE European Test Workshop, Cagliari (Grand Hotel Chia Laguna), Italy, May 28 - 30, 1997.

"Using Commercial ATPG Tools to Accurately Predict and Minimize Defective Part Level," (with J. Dworak, M. R. Grimaila, J. Wicker, K. M. Butler, B. Stewart, L-C. Wang, and T. W. Williams), Eighth International Test Synthesis Workshop, Santa Barbara, CA, March 26 - 28, 2001.

"A Study of Gate-Level Modeling Biases in DFT Methodologies for Testing Custom Designs," (with L-C. Wang, and M. S. Abadir), Eighth International Test Synthesis Workshop, Santa Barbara, CA, March 26 - 28, 2001.

"A Statistical Analysis of the Sensitivity to Defective Part Level Model Parameters during Test Pattern Set Selection (with J. Dworak, M. Grimaila, K. Butler, Jason Wicker and B. Stewart), The Ninth International Test Synthesis Workshop, Santa Barbara, CA, March 25 - 27, 2002. (**Best Student Presentation Award of the Ninth ITSW – student presenting was Jennifer Dworak**)

"The Effect of Uncertainty in the Model Parameter Tau on the Effectiveness of Test Sets Optimized with MPG-D," (with J. Dworak, M.R. Grimaila, J. Wingfield, B. Cobb, S. Lee, J. Wicker, K. Butler, B. Stewart, and B. Underwood), 3rd IEEE International Workshop on Microprocessor Test and Verification, Austin, TX, June 6-7, 2002.

"A New Estimator for Mean Time to First Failure: How Bad Were Those Defective IC's We Missed?" (with J. Dworak, D. Dorsey, and A. Wang), Tenth International Test Synthesis Workshop, Santa Barbara, CA, March 31-April 2, 2003.

"Evaluating a Greedy ATPG Algorithm for Generating Compact Transition Test Sets in Accordance with the Principles of DO-RE-ME," (with S. Lee, J. Dworak, and B. Cobb), 4th International Workshop on Microprocessor Test and Verification, Austin, TX, May 29-30, 2003.

"Binary Decision Diagrams and their Applications in Manufacture Testing," (with J. Wingfield, and B. Cobb), Eleventh International Test Synthesis Workshop, Santa Barbara, CA, April 5 - 7, 2004.

"Defect Delectability Classes and Their Effect on Optimal Test Pattern Generation Strategies," (with J. Dworak), Eleventh International Test Synthesis Workshop, Santa Barbara, CA, April 5 - 7, 2004.

"Reducing Structural Bias: An Initial Look at Observation Diversity," (with J. Dworak and J. Wingfield), Fifth International Workshop on Microprocessor Test and Verification, Austin, TX, September 8 - 10, 2004.

INVITED LECTURES:

"Computer-Aided Testing and Simulation," First Annual Research Review, Department of Electrical and Computer Engineering, The University of Texas at Austin, May 8, 1984.

"Automatic Test Pattern Generation for Digital Logic Circuits," Second Annual Research Review, Department of Electrical and Computer Engineering, The University of Texas at Austin, May 7, 1985.

"Computer-Aided Testing and Simulation," Texas Instruments, Dallas, TX, June 1985.

"New Directions in Logic Design for Testability," International Business Machines Corporation, Purchase, NY, April 8, 1986.

"New Directions in Logic Design for Testability," Semiconductor Research Corporation, Research Triangle Park, NC, April 11, 1986.

"Research in Logic Testing at the University of Texas at Austin," Weekly Undergraduate Seminar, Mississippi State University, Columbus, MS, November 6, 1986.

"New Issues in Design for Testability," Stanford University, Stanford, CA, November 18, 1986.

"New Issues in Design for Testability," Tektronix Research Laboratories, Beaverton, OR, November 19, 1986.

"Some New Results Using Structured Logic Design Methods," McGill University, Montreal, Quebec, Canada, March 10, 1987.

"A New Design for Testability Method," General Electric Central Research and Development Laboratories, Schenectady, NY, April 9, 1987.

"The Value of Endowed Funds for Research at The University of Texas at Austin," Endowed Donors Dinner, February 26, 1988.

"The Boolean Difference from a New Perspective," The Technical University of Trondheim, Trondheim, Norway, March 17, 1988.

"Automatic Test Pattern Generation for Digital Logic Circuits," IEEE Computer Society, The University of Texas at Austin, April 6, 1988.

"Automatic Test Pattern Generation for Digital Logic Circuits," Schlumberger Austin Systems Center, Austin, Texas, April 7, 1988.

"Automatic Test Pattern Generation for Digital Systems," AT&T, Murray Hill, New Jersey, April 15, 1988.

"An Empirical Comparison of Random-Pattern Testability Under Two Classes of Delay Fault Coverage," NCR Technical Information Exchange Session, MCC, Austin, Texas, May 4, 1988.

"Designing and Testing Integrated Circuits," The Honors Colloquium, The University of Texas at Austin, July 26, 1985, July 26, 1986, July 25, 1987, July 22, 1988, and July 22, 1989.

"Statistical Delay Fault Coverage and Defect Level for Delay Faults," IBM, Austin, Texas, September 22, 1988.

"Statistical Delay Fault Coverage and Defect Level for Delay Faults," Northeastern University, Boston, MA, March 9, 1989.

"Results from a Survey of Electronic Board Testing Methods," Digital Equipment Corporation, Andover, MA, September 18, 1990.

"Design Verification and Testing -- A Functional Perspective," Massachusetts Institute of Technology VLSI Seminar, Cambridge, MA, November 20, 1990.

"Design Verification and Testing -- A Functional Perspective," MCC, Austin, TX, December 4, 1990.

"Design Verification and Testing -- A Functional Perspective," Philips Research Laboratories, Eindhoven, The Netherlands, March 1, 1991.

"Design Verification and Testing -- A Functional Perspective," University of Virginia, Charlottesville, VA, July 19, 1991.

"All Tests are not Equally Valuable for Non-Target Defect Detection," Center for Reliable Computing, Stanford University, Stanford, CA, November 13, 1992.

"All Tests are not Equally Valuable for Non-Target Defect Detection," Center for Reliable Computing, Stanford University, Stanford, CA, November 13, 1992.

"New Testing Methods to Enhance Defect Detection using Existing Fault Models and CAD Tools," Computer Engineering Seminar, University of Illinois at Urbana-Champaign, April 15, 1997.

"The Beginning of the End for Stuck-at-Fault Based Testing," Computer-Aided Design Seminar, University of California at Berkeley, October 23, 1997.

"A New Model for Defective Part Level Estimation and its Impact on Automatic Test Pattern Generation," Texas Instruments, Dallas, TX, January 30, 1998.

TUTORIALS:

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), 27th Design Automation Conference Tutorial, Orlando, FL, June 28, 1990.

"Logic Testing and Design for Testability," Rockwell Testing Conference, Newport Beach, CA, January 17, 1991.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), European Test Conference Tutorial, Munich, Germany, April 10-12, 1991.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), 5th Annual European Computer Conference Tutorial, Bologna, Italy, May 13-16, 1991.

"Introduction to Integrated Circuit Design" Motorola (William Cannon Site), Austin, Texas, December 3, 5, 9, and 10 1991.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), Nordic Workshop on Design Verification and Test, Roros, Norway, March 11, 1992.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, April 28-May 1, 1992.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), 29th Design Automation Conference Tutorial, Anaheim, CA, June 12, 1992.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, September 1, 3, 8, and 10 1992.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), International Test Conference Tutorial, Baltimore, MD, September 20, 1992.

"Introduction to Integrated Circuit Design" Motorola (William Cannon Site), Austin, Texas, December 14-17, 1992.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), International Test Conference Tutorial, Baltimore, MD, September 20, 1992.

"Testing Digital Circuits and Design for Test," (with T. W. Williams), IEEE International ASIC Conference Tutorial, Rochester, NY, September 28, 1993.

"Techniques for Designing More Testable Logic Networks," (with T. W. Williams), International Test Conference Tutorial, Baltimore, MD, October 17, 1993.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, September 21-24, 1993.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, November 29 - December 2, 1993.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, March 21 - March 24, 1994.

"Introduction to Integrated Circuit Design" Motorola (William Cannon Site), Austin, Texas, April 5 - April 8, 1994.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, June 28 - July 1, 1994.

"Introduction to Integrated Circuit Design" Motorola (Ed Bluestein Site), Austin, Texas, September 13-16, 1994.

"Testing Digital Circuits and Design Using Scan and Self-Test," (with T. W. Williams), IEEE International ASIC Conference Tutorial, Rochester, NY, September 19-23, 1994.

PATENTS:

"Scan Testable Integrated Circuit" (with V. D. Agrawal), Patent 4,493,077, United States Patent and Trademark Office, issued January 8, 1985.

"Universally Testable Logic Elements and Method for Structural Testing of Logic Circuits Formed of Such Logic Elements," Patent 4,625,310, United States Patent and Trademark Office, issued November 25, 1986.

GRANTS AND CONTRACTS:

University Research Institute, "A New Automatic Test Generation Algorithm," April-August, 1983, \$2,136.

Hewlett-Packard Equipment Grant, 1984, \$2,800.

Bureau of Engineering Research, "Generalized Graph Operations for CAD Systems," 1984, \$3,000.

Microelectronics and Computer Technology Corporation, "Rule Based Automatic Test Pattern Generation Using Boolean Difference Concepts," January 1 - December 31, 1985, \$48,976.

GE Calma, "Software License for the TEGAS Logic Simulator," May, 1983 - August, 1986, \$135,000 commercial value.

AT&T Information Systems, "Automatic Testing for Faults in Digital Systems," January 1, 1985 - August 31, 1986, \$25,000.

Microelectronics and Computer Technology Corporation, "Test Generation for Faults," January 1 - December 31, 1986, \$25,000.

International Test Foundation, "Automatic Test Pattern Generation for Delay Faults in Digital Logic Circuits," September 1, 1986 - August 31, 1987, \$14,592.

AT&T Information Systems, "Fault Detection in Digital Systems", May 1, 1986 - December 31, 1987, \$30,000.

Microelectronics and Computer Technology Corporation, "Continuation of Testing Research," January 1 - December 31, 1987, \$25,000.

AT&T Information Systems, "Continuation of Fault Detection Research," May 1, 1987 - December 31, 1988, \$25,000.

International Test Foundation, "Test Technology in the Electrical Engineering Curriculum," January 1, 1988 - July 1, 1989, \$30,985. (\$10,153 for NSF Matching)

Microelectronics and Computer Technology Corporation, "Continuation of Testing Research," January 1 - December 31, 1988, \$25,000.

Microelectronics and Computer Technology Corporation, "Testable System Design of Digital Systems and Knowledge Based Structures," (with Xi-an Zhu) April 1, 1988 - March 31, 1989, \$92,750.

Office of Naval Research, "Fault-Tolerant Design Techniques for Advanced Digital Architectures" (with M. Malek), Contract #N00014-86-K-0554, July 1, 1986 - December 31, 1988, \$180,000.

National Science Foundation Presidential Young Investigator Award, Grant #MIPS-8552537, June 1, 1986 - May 31, 1991, up to \$500,000 (with matching industrial funds).

AT&T Information Systems, "Topological Testing," September 1, 1988 - August 31, 1989, \$25,000.

Semiconductor Research Corporation, "The Design of Testable Systems" (with J. Abraham, J. Rahmeh and W. Rogers), SRC Contract, September 1, 1988 - August 31, 1989, \$20,000.

Office of Naval Research, "Testing and Fault-Tolerant Design Techniques for Advanced Digital Architectures" (with M. Malek), Contract #N00014-86-K-0554, January 1, 1989 - December 31, 1991, \$240,000.

Semiconductor Research Corporation, "The Design of Testable Systems" (with J. Abraham, J. Rahmeh and W. Rogers), SRC Contract #88-DJ-142, January 15, 1989 - January 14, 1990, \$250,000.

IBM Corp., "Electronic Testing -- Department Grant" (with J. Abraham), August 1, 1989 - July 31, 1992, \$75,000.

Cimflex Teknowledge, "Knowledge Based Design for Testability" (with Xi-an Zhu), June 13 - December 31, 1989, \$28,015.

Microelectronics and Computer Technology Corporation, "Continuation of Testing Research," December 7, 1989 - December 31, 1990, \$5,000.

Semiconductor Research Corporation, "The Design of Testable Systems" (with J. Abraham, J. Rahmeh, W. Rogers, and L. Pillage), SRC Contract #90-DP-142, January 15, 1990 - January 14, 1991, \$350,000.

Texas Advanced Technology Program, "Refined Models of Integrated Circuit Defects Inducing Additional Delays," (with Lawrence T. Pillage), April 24, 1990 - August 31, 1991, \$ 137,922.

Semiconductor Research Corporation, "The Design of Testable Systems" (with J. Abraham, J. Rahmeh, W. Rogers, and L. Pillage), SRC Contract #91-DP-142, January 15, 1991 - August 31, 1992, \$585,000.

Motorola, Inc., "Timing Analysis for Integrated Circuits," (with Lawrence T. Pillage), November 29, 1991 - December 31, 1992, \$10,000.

Office of Naval Research, "Enhanced Timing Analysis for Reliable Wafer Scale Integrated Systems," Contract #N00014-92-J-1723, May 1, 1992 - April 30, 1995, \$300,000.

Semiconductor Research Corporation, "The Design of Testable Systems" (with J. Abraham, W. Rogers, and L. Pillage), SRC Contract #92-DP-142, September 1, 1992 - August 31, 1993, \$370,000.

Advanced Research Projects Agency (ARPA), "A Unified CAD Tool for Integrated Systems," (with Dean Neikirk and Lawrence T. Pillage) DAAL01-93-K-3317, February 26, 1993 - February 26, 1995, \$648,069.

Semiconductor Research Corporation, "The Design of Testable Systems" (with J. Abraham), SRC Contract #93-DP-142, September 1, 1992 - August 31, 1993, \$270,000.

National Science Foundation, "ARI: Development of a Novel Systems Software for Multimedia and High-Performance Computing," Reddy, Mercer, Lu, Cantrell, and Choi, September 15, 1996 - August 31, 1999, \$127,450, (Equipment grant).

Texas Advanced Technology Program, "Defect-Directed Test Pattern Generation for Manufacture Testing of Integrated Circuits," January 1, 1998 - December 31, 1999, \$139,491.

Semiconductor Research Corporation Custom Research Proposal Sponsored by Texas Instruments, "Automatic Test Pattern Generation for Defect-Directed At-Speed Testing," (with Mike Grimaila) August 1, 2000 - July 31, 2003, \$165,000.

U. S. Department of Education, "Meeting the Purposes of Authorizing Statue," (with N. Reddy and K. Watson) August 1, 2001 - July 31, 2004, \$ 327,600.

IBM Faculty Partnership Award, "Novel Techniques for Quantifying Confidence during Multi-Processor Verification, Validation, Debug, and Diagnosis," August 1, 2001 - July 31, 2002, \$ 25,000.

AMD Research Support Grant, "Integrated Circuit Testing," November 1, 2001 – October 31, 2002, \$ 8,000.

Texas Advanced Technology Program, "Integrating Design Verification Techniques with Defect-Oriented ATPG for Very Deep Submicron Systems," April 18, 2002 - December 31, 2003, \$139,720.

IBM Faculty Partnership Award, "A New Approach During Multi-Processor Verification and Validation for Estimating Design Correctness," August 1, 2002 - July 31, 2003, \$ 25,000.

IBM Faculty Partnership Award, "Quantifying Design Correctness during Multi-Processor Verification and Validation," August 1, 2003 - July 31, 2004, \$ 25,000.

IBM Faculty Partnership Award, "A Study of AC Timing Defects: Test Pattern Quality and its Relationship to Real-Time System Errors," August 1, 2004 - July 31, 2005, \$ 25,000.

COURSES AT TEXAS A&M UNIVERSITY:

<u>Semester</u>	<u>Course #</u>	<u>Course Title</u>
Fall 2004	EE 680	Testing and Diagnosis of Digital Systems
Fall 2003	EE 652	Switching Theory
Spring 2003	EE 248	Introduction to Digital Logic Design
Spring 2002	EE 248	Introduction to Digital Logic Design
Spring 2001	EE 248	Introduction to Digital Logic Design
Fall 2000	EE 652	Switching Theory
Spring 2000	EE 248	Introduction to Digital Logic Design
Fall 1999	EE 680	Testing and Diagnosis of Digital Systems
Spring 1999	EE 248	Introduction to Digital Logic Design
Fall 1998	EE 652	Switching Theory
Spring 1998	EE 248H	Introduction to Digital Logic Design -- Honors
Fall 1997	EE 680	Testing and Diagnosis of Digital Systems
Spring 1997	EE 248	Introduction to Digital Logic Design
Fall 1996	EE 652	Digital Systems Design
Spring 1996	EE 248	Introduction to Digital Logic Design
Fall 1995	EE 680	Testing and Diagnosis of Digital Systems

COURSES AT THE UNIVERSITY OF TEXAS AT AUSTIN:

<u>Semester</u>	<u>Course #</u>	<u>Course Title</u>
Spring 1995	EE 382M	Topics in Design Verification and Testing
Spring 1994	EE 360M	Digital Systems Engineering II
Fall 1993	EE 382L	Switching Theory
Spring 1993	EE 360M	Digital Systems Engineering II
Fall 1992	EE 382M	Fault Tolerant Computing I
Spring 1992	EE 360M	Digital Systems Engineering II
Fall 1991	EE 382L	Switching Theory
Spring 1991	EE 360M	Digital Systems Engineering II

Fall	1990	EE 382L	Switching Theory
Spring	1990	EE 382M	Fault Tolerant Computing I
Fall	1989	EE 382L	Switching Theory
Spring	1989	EE 382M	Fault Tolerant Computing I
Fall	1988	EE 382L	Switching Theory
Spring	1988	EE 382M	Fault Tolerant Computing I
Fall	1987	EE 382L	Switching Theory
Fall	1987	EE 360M	Digital Systems Engineering II
Spring	1987	EE 382M	Fault Tolerant Computing I
Spring	1986	EE 382M	Fault Tolerant Computing I
Spring	1986	EE 360M	Digital Systems Engineering II
Fall	1985	EE 382L	Switching Theory
Spring	1985	EE 382M	Fault Tolerant Computing I
Fall	1984	EE 382L	Switching Theory
Fall	1984	EE 360M	Digital Systems Engineering II
Spring	1984	EE 382M	Fault Tolerant Computing I
Spring	1984	EE 382M	Fault Tolerant Computing I
Fall	1983	EE 382L	Switching Theory
Summer	1983	EE 382L	Computer Logic Simulation
Spring	1983	EE 360M	Digital Systems Engineering II

PH.D. SUPERVISIONS COMPLETED:

Thomas E. Kirkland	1986	University of Texas at Austin
Ki Soo Hwang	1986	University of Texas at Austin
Rhonda Gaede	1988	University of Texas at Austin
C. T. Glover	1989	University of Texas at Austin
Eun Sei Park	1989	University of Texas at Austin
Kenneth Butler	1990	University of Texas at Austin
Don Ross	1990	University of Texas at Austin
Bret Stewart	1990	University of Texas at Austin
Rohit Kapur	1992	University of Texas at Austin
Mark Heap (with W. A. Rogers)	1993	University of Texas at Austin
Ronn Brashear	1994	University of Texas at Austin
Jaehong Park	1995	University of Texas at Austin
Chanhee Oh	1995	University of Texas at Austin
Li-Chung Wang	1996	University of Texas at Austin
Steve Smith	1996	University of Texas at Austin

Mike Grimaila August 1999 Texas A&M University
*Maximizing Non-Target Defect Detection Using Conventional
Stuck-at Fault-Based Automated Test Pattern Generation Tools*

Sooryong Lee August 2003 Texas A&M University
*A New ATPG Algorithm to Generate a Compact Test Sets Which
Detect Static and Dynamic Defects in VLSI Circuits*

Jennifer Dworak May 2004 Texas A&M University
*Modeling Defective Part Level Due to Static and Dynamic
Defects Based upon Site Observation and Excitation Balance*

M.S. SUPERVISIONS COMPLETED:

Dong Whoan Kim	1984	University of Texas at Austin
Hosung Kim	1984	University of Texas at Austin
Eric J. Schell	1984	University of Texas at Austin
James McKenzie	1985	University of Texas at Austin
Rhonda Gaede	1986	University of Texas at Austin
Ken Butler	1987	University of Texas at Austin
Steve McMahan	1987	University of Texas at Austin
Yi-Feng Lin (Report)	1988	University of Texas at Austin
Tarak M. Parikh	1988	University of Texas at Austin
Wilburn Underwood	1988	University of Texas at Austin
Chih-Teng Hung	1989	University of Texas at Austin
Marvin Denman	1990	University of Texas at Austin
Mark Naiver	1993	University of Texas at Austin
David Carlson	1994	University of Texas at Austin

Mehler, Ronald W.	September	1998	Texas A&M University
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Koh, T-Pinn Ronnie	December	1998	Texas A&M University
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Jennifer Dworak (Texas A&M University Honors Program 1997-1998)	May	2000	Texas A&M University
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Jason Wicker <i>An Analysis of Test Effectiveness via Surrogate Simulation of a Commercial IC</i>	December	2001	Texas A&M University
--	----------	------	----------------------

Michael Trinka <i>Defect Site Prediction Based Upon Statistical Analysis of Fault Signatures</i>	August	2003	Texas A&M University
---	--------	------	----------------------

Bradley Douglas Cobb (Texas A&M University Honors Program 2000-2001) <i>Ordered Partial Decision Diagrams and their use in Manufacture-Test Generation</i>	December	2003	Texas A&M University
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David Dorsey (Texas A&M University Honors Program 2001-2002) <i>Estimating the Expected Latency to Failure Due to Manufacturing Defects</i>	December	2003	Texas A&M University
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James Wingfield <i>Approaches to Test Set Generation using Binary Decision Diagrams</i>	December	2003	Texas A&M University
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TEXAS A&M UNIVERSITY UNDERGRADUATE HONORS RESEARCH PROJECT SPONSOR:

Jennifer Dworak	1998	Best Student Presentation Award
Brad Cobb	2000	Best Student Presentation Award
David Dorsey	2002	Best Paper Award
Jeff Cobb	2003	
Jason Vanfickell	2003	
Nate Davis	2004	

PREVIOUS UNDERGRADUATE RESEARCH STUDENTS:

Theresa Huth	Spring 2003 (Winner of an Undergraduate Student Research Best Oral Presentation Award)
Adam Skelton	(Winner of the Thomas S. Gathright Academic Excellence Award Top Junior in the College of Engineering for 2000 - 2001)
John Lee	Fall 2003 & Spring 2004
Cynthia McReynolds	Summer 2003 & Fall 2003
William Charles Price	Fall 2003 & Spring 2004
Justin Ray	Summer 2003 & Fall 2003
Jason Vanfickell	Summer 2003, Fall 2003 & Spring 2004
Jeff Cobb	Fall 2003 & Spring 2004 & Fall 2004
Nate Davis	Fall 2003 & Spring 2004

POST DOCTORAL RESEARCHERS:

Xian Zhu	1988 -- 1990
Kenneth Butler	1990 (Fall)
Don Ross	1990 -- 1991
Mike Grimaila	1999 -- 2001
Jennifer Dworak	2004 (Summer and Fall)

SHORT BIOGRAPHY:

M. Ray Mercer is a Professor Emeritus of Electrical and Computer Engineering at Texas A & M University. In September of 2005 he retired as Professor of Electrical and Computer Engineering, Leader of the Computer Engineering Group, and holder of the Computer Engineering Chair. His research interests are centered in computer engineering and include: the computer-aided design of digital systems, design verification, simulation, design for testability, the modeling of logic networks, automatic test pattern generation, distributed computation, communications, and fault-tolerant computing.

Previously, Dr. Mercer worked at: The University of Texas, Austin, TX; AT&T Bell Laboratories, Murray Hill, NJ; Hewlett-Packard Laboratories, Palo Alto, CA; and General Telephone and Electronics, Mountain View, CA. He holds a B.S.E.E. from Texas Tech University, an M.S.E.E. from Stanford University, and a Ph.D. in Electrical Engineering from The University of Texas at Austin. He was the Program Chairman for the 1989 International Test Conference and holds two patents in design for testability. Mercer became a National Science Foundation Presidential Young Investigator in 1986; he has won Best Paper Awards at the International Test Conference (in 1982), the Design Automation Conference (in 1991), and the VLSI Test Symposium (in 1999); he is a Fellow of the Institute of Electrical and Electronics Engineers.

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